IL04/915

מדינת ישראל
STATE OF ISRAEL

Ministry of Justice
Patent Office

משרד המשפטים
לשכת הפטנטים

This is to certify that annexed hereto is a true copy of the documents as originally deposited with the patent application particulars of which are specified on the first page of the annex.

זאת לתעודה כי רצופים בזה העתקים נכונים של המסמכים שהופקדו לכתחילה עם הבקשה לפטנט לפי הפרטים הרשומים בעמוד הראשון של הנספח.

This 27-10-2004 היום

ש. לשרי
ממונה על הבוחנים

רשם הפטנטים
Commissioner of Patents

נתאשר
Certified

חוק הפטנטים, תשכ"ז — 1967
PATENTS LAW, 5727-1967

בקשה לפטנט
Application For Patent

לשימוש הלשכה
For Office Use

158345	מספר: Number
09-10-2003	תאריך: Date
	הוקדם/נדחה: Ante/Post-dated

אני, (שם המבקש, מענו ולגבי גוף מאוגד - מקום התאגדותו)
I, (Name and address of applicant, and in case of body corporate-place of incorporation)

Interon AS of
Ringveien 14
N-1386 Asker
NORWAY

בעל אמצאה מכח הדין Right of Law ששמה הוא
Owner, by virtue of Right of Law of an invention the title of which is

(בעברית) (Hebrew)

גלאי הכולל מערך פיקסלים ותהליך ייצור והרכבה שלו

(באנגלית) (English)

Pixel detector and method of manufacture and assembly thereof

מבקש בזאת כי ינתן לי עליה פטנט
Hereby apply for a patent to be granted to me in respect thereof.

* בקשת חלוקה Application of Division	* בקשת פטנט מוסף Appl. for Patent of Addition	* דרישת דין קדימה Priority Claim		
מבקשת פטנט from application	* לבקשה/לפטנט to Patent/Appl.	מספר/סימן Number/Mark	תאריך Date	מדינת האיגוד Convention Country
No. ______ מס'	No. ______ מס'			
Dated מיום	Dated מיום			
P.O.A.: * יפוי כח: עוד יוגש				
המען למסירת מסמכים בישראל Address for Service in Israel C. 148614 REINHOLD COHN AND PARTNERS ריינהולד כהן ושותפיו Patent Attorneys עורכי פטנטים P.O.B. 4060, Tel-Aviv ת"ד 4060, תל-אביב				

חתימת המבקש
Signature of Applicant

For the Applicants,
REINHOLD COHN AND PARTNERS
By : —

This היום 9 of בחודש October Year שנת 2003

לשימוש הלשכה
For Office Use

טופס זה כשהוא מוטבע בחותם לשכת הפטנטים ומושלם במספר ובתאריך ההגשה, הנו אישור להגשת הבקשה שפרטיה רשומים לעיל.
This form, impressed with the Seal of the Patent Office and indicating the number and date of filing, certifies the filing of the application the particulars of which are set out above.

* מחק את המיותר
Delete whatever is inapplicable

גלאי הכולל מערך פיקסלים ותהליך ייצור והרכבה שלו

Pixel detector and method of manufacture and assembly thereof

Interon AS

C. 148614

Pixel detector and method of manufacture and assembly thereof

FIELD OF THE INVENTION

This invention relates to pixel sensors for use in X-ray and γ-cameras.

BACKGROUND OF THE INVENTION

Pixel sensors are known to comprise an array of sensor elements such as diodes, and a complementary array of electronics, typically in the form of an ASIC and comprising a charge amplifier and processing electronics for each sensor element. In CCDs such as are used in miniature television cameras and the like, the sensor elements are formed of silicon diodes which are responsive to visible light for producing a current which is amplified by the charge amplifier and subsequently processed.

Pixel sensors for X-ray and nuclear medical imaging are known that respond to high-energy photons such as X-rays or γ-rays and produce charge in a similar manner. Conventional silicon diodes are not suitable for such applications because they are transparent to the high-energy photons and therefore other materials such as cadmium telluride or mercury iodide are used instead. Since these materials are not based on silicon, the diode cannot be integrated together with the associated electronics as a single monolithic structure and this requires, in practice, that the sensor elements and the associated electronics be manufactured on separate wafers, which are then interconnected using bump bonding.

Our prior application PCT/IL03/00125 entitled "*Pixel sensor array and method of manufacture thereof*" and filed February 18, 2003 discloses a sensor array having a plurality of pixels formed on a wafer 10 as shown in Fig. 1. The wafer 10 constitutes an integrated circuit or chip, typically formed of a complementary metal oxide semiconductor (CMOS) wafer and provided with scribe lines 11 so as to form a rectangular matrix of sensor elements 12 each of which, in turn, comprises a matrix of 3 x 5 pixels 13. The wafer 10 is processed at a silicon foundry in known manner and for the purpose of low-cost mass-production is processed according to the invention as an uncut wafer bearing multiple replicas of the same integrated circuit. Each pixel 13 includes a sensor input 14 that is connected to a charge amplifier 15 and a processing unit 16. The charge amplifier 15 together with the processing unit 16 constitute the pixel electronics to which the sensor element (not shown) is connected and which responds to a photon striking the sensor element for measuring the charge produced thereby. Thus, the silicon wafer 10 contains multiple replicas of the pixel array 12 which, after scribing, would produce multiple ASICs each containing an array of 3 x 5 pixel electronic circuits for connecting to a respective sensor element.

In order to obviate the need for wire bonding as commonly used in pixel sensors, PCT/IL03/00125 connects each sensor input 14 via a respective ohmic contact (or "via") through the silicon wafer to the reverse side thereof. This contact may then be used to connect the sensor element directly to the sensor electronics by effectively bonding the sensor element in correct spatial disposition with respect to the electronics on the reverse side of the silicon wafer.

Fig. 2 shows pictorially a typical arrangement comprising a standalone 2-D pixel sensor depicted generally as 20 and comprising an upper sensor array 21 comprising multiple sensor elements (not shown), each of which is bump-bonded to a corresponding electronics module in a lower ASIC 22. In addition, power and control signals are fed to the sensor 20 and this typically requires that control-pads 23 be formed along at least one edge of the composite chip and which may be connected to external circuitry using wire-bonding 24.

The typical size of each pixel in such an array is 200 μm and the typical dimensions of the two-dimensional array is 1 cm^2. This means that there are typically some 625 pixels per pixel array. In practice, it is usually necessary to image over a much larger area, for example at least 10 x 10 cm^2. This requires that 100 pixel arrays must be packed together, for example as a 10 x 10 matrix. On the one hand, the bump bonding technique used in conventional pixel sensors militates against the closer packing density of the pixels so that it becomes difficult to increase the resolution of the sensor by packing more pixels into a pixel array, since the need to bump-bond each sensor to the corresponding electronics in a different array is a costly process and is subject to low yields. Furthermore, the provision of control-pads along an edge of each module and the need to wire bond these pads to external circuitry means that adjacent sensor arrays cannot be packed edge-to-edge without introducing a "dead" zone where there are, in fact, no pixels at all owing to the interposing I/O and control-pads. Moreover, the connection of the I/O control-pads to the external circuitry by wire bonding is also a costly and cumbersome process and further reduces the effective overall packing density.

US 5,254,868 (Yutaka) published October 19, 1993 and entitled "*Solidstate image sensor device*" discloses a semiconductor image sensor device comprising arrayed photo-sensors, wherein a connection electrode used for connecting an external circuit or an aperture on the connection electrode is provided at an opposite side surface to an illuminated surface, and a transparent substrate is provided above the arrayed photo-sensors. By such means the distance between a light source and the photo-sensors can be reduced so as to improve sensitivity and resolving power.

US 5,998,292 (Black *et al.*) issued Dec. 7, 1999 and entitled "*Method for making three dimensional circuit integration*" discloses a method for inter-connecting, through high-density micro-post wiring, multiple semiconductor wafers with lengths of about a millimeter or below. The method comprises etching at least one hole, defined by walls, at least partly through a semiconducting material;

forming a layer of electrically insulating material to cover said walls; and forming an electrically conductive material on said walls within the channel of the hole.

JP 61 128564A2 (Fujitsu Ltd.) published Jun. 16, 1986 and entitled "*Semiconductor Device*" describes a process for forming a photodetecting section and a driving circuit on the surface and the back of the same substrate and connecting both by a wiring through a through-hole. An amplifier and other driving circuits are shaped to a Si growth layer, and an n type region is formed through the implantation of B+ ions in order to shape a P-N junction for a photodetecting element. Aluminum for a wiring is shaped so as to unit one part of the n type region and the Si growth layer side where the driving circuit is formed, and shaped through a method, such as ion beam evaporation, electron beam evaporation, etc. while masking sections except a required section. Aluminum is evaporated from both upper and lower surfaces, and the wiring is connected by plating. A HgCdTe growth section in the photo-detecting element section and the Si growth layer are displaced, and formed on both surfaces of a sapphire substrate.

Such a configuration appears to relate to a single photo-detector only and the silicon is not pre-fabricated but rather is grown on top of the sapphire substrate.

EP1 045 450A2 (Agilent Technologies Inc.) published Oct. 18, 2000 and entitled "*Image sensor array device*" discloses an image sensor array that includes a substrate. An interconnect structure is formed adjacent to the substrate. An amorphous silicon electrode layer is adjacent to the interconnect structure. The amorphous silicon electrode layer includes electrode ion implantation regions between pixel electrode regions. The pixel electrode regions define cathodes of an array of image sensors. The electrode ion implantation regions provide physical isolation between the pixel electrode regions. The cathodes are electrically connected to the interconnect structure. An amorphous silicon I-layer is adjacent to the amorphous silicon electrode layer. The amorphous silicon I-layer forms an inner layer of each of the image sensors. A transparent electrode layer is formed adjacent to the image sensors. An inner surface of the transparent electrode layer is electrically connected to anodes of the image sensors and the interconnect structure.

The amorphous silicon I-layer can further include I-layer ion implantation regions that provide physical isolation between the inner layers of the image sensors. The I-layer ion implantation regions align with the electrode ion implantation regions. An amorphous silicon P-layer can be formed adjacent to the amorphous silicon I-layer. The amorphous silicon P-layer forms an outer layer of each of the image sensors. The amorphous silicon P-layer can include P-layer ion implantation regions that provide physical isolation between the outer layers of the image sensors.

EP 537 514A2 (Mitsubishi corporation) published Apr. 21, 1993 and entitled "*Optoelectronic integrated circuit*" discloses an optoelectronic integrated circuit including a light receiving element for converting an optical signal to an electric signal and an electronic circuit for processing the electric signal. The light receiving element is disposed on a first main surface of the substrate and includes p side electrodes and n side electrodes alternately arranged in parallel to each other. The electronic circuit is disposed on a second main surface of the substrate. The light receiving element is electrically connected to the electronic circuit by a via hole penetrating through the substrate.

US 4,547,792 (Sclar) issued Oct. 15, 1985 and entitled "*Selective access array integrated circuit*" discloses a semiconductor integrated circuit having an array of electronic devices and a plurality of electronic access devices. The access devices consist of sets of MOSFETs which may be turned on by the joint action of X and Y address lines to permit individual and isolated electrical connection between selected electronic devices in the array and peripheral on or off-chip sensing circuits. This permits continuous readout to be established and maintained for the selected devices without interference with the other devices in the array and without a requirement to readout any but the selected devices. In order to provide minimum dead space between the array detectors, the array and access devices may be disposed on opposite surfaces of the semiconductor body.

US 4,857,746 (Werner *et al.*) issued Aug. 15, 1989 and entitled "*Method for producing an optocoupler*" discloses a method for manufacturing optocouplers or reflex light barriers, wherein semiconductor light transmitters and semiconductor

light receivers are situated on a single substrate. The optic coupling or optic isolation of light transmitter and light receiver takes place in the substrate. Only then are semiconductor elements separated into discrete units.

Regardless of what technology is used to fabricate the sensor array, and regardless of the size of the sensor array, a practical CT detector always requires that multiple sensor array be juxtaposed edge to edge in order to provide adequate coverage. Inevitably this introduces some "dead space" between adjacent sensor arrays which is insensitive to incoming photons as discussed above. It is clearly desirable to reduce the dead space as much as possible. The small size of hitherto-proposed sensor arrays such as shown in Fig. 2 having contact pads at an edge on the one hand militates against their use as standalone X-ray or γ-ray detectors and, on the other hand, renders it inevitable that when juxtaposed edge to edge there will be created dead spaces in the central regions of the detector which are insensitive to incoming photons.

Our PCT/IL03/00125 as well as some of the other references discussed above address this problem and provide one solution: namely the provision of conductive vias so that connections to the sensor elements can be effected through the reverse side of the wafer. This solution is effective but the need to provide the conductive vias complicates the manufacturing process.

It would therefore be desirable to provide an alternative solution that obviates the need to provide conductive vias through the silicon wafer, but nevertheless permits multiple sensor arrays to be juxtaposed without creating the dead space associated with know approaches.

SUMMARY OF THE INVENTION

It is thus an object of the invention to provide a pixel sensor array that obviates the need to provide conductive vias through the silicon wafer, but nevertheless permits multiple sensor arrays to be juxtaposed without creating dead space in the central regions of the detector.

This object is realized in accordance with the invention by a method for fabricating a detector assembly having multiple juxtaposed sensor arrays each having a plurality of pixels that include a sensor element coupled to a sensor input of an electronic processing circuit, the method comprising:

integrating the electronic processing circuits on a very large area CMOS wafer having a major edge and a minor edge, the major having a dimension that is no less than approximately half of a width of the detector so as to form an integrated circuit having at least one array of electronic processing circuits each electronic processing circuit having a respective sensor input disposed toward a first surface of the wafer and accessible from the first surface via a contact formed towards a minor edge of the sensor array;

juxtaposing multiple pairs of sensor arrays edge to edge so that respective minor edges of each of pair are juxtaposed with the respective contacts of each sensor array disposed toward opposing outer non-contiguous edges of the detector and with adjacent pairs of sensor arrays being juxtaposed along their major edges; and

disposing the sensor elements on the first surface of the respective integrated circuits in said detector assembly whereby an exposed surface of the sensor elements forms a common first electrode towards which incident photons are directed, and an opposite unexposed surface thereof forms multiple second electrodes of opposite polarity to the first electrode each in registration with a corresponding sensor input.

The invention is based on the use of CMOS ICs having a very large surface area, typically an order of magnitude larger than those used hitherto in the manufacture of sensor arrays. This is a new fabrication process that allows CMOS to be integrated in larger wafer size. Thus, for example, while conventional CMOS wafers have a major dimension of at most several centimeters, CMOS wafers manufactured according to this technology may have a stitched reticle size exceeding 10 cm and this is likely to increase in the near future.

BRIEF DESCRIPTION OF THE DRAWINGS

In order to understand the invention and to see how it may be carried out in practice, a preferred embodiment will now be described, by way of non-limiting example only, with reference to the accompanying drawings, in which:

Figs. 1and 2 show pictorially prior-art pixel sensor assemblies;

Fig. 3 shows pictorially an exploded view of a sensor array that is mass-manufactured on a silicon wafer in a first manufacturing step according to the invention;

Fig. 4 shows pictorially the fabricated sensor array after completion of the first manufacturing step;

Fig. 5 shows pictorially a plurality of sensor arrays being juxtaposed so as form a detector in a second manufacturing step;

Fig. 6 shows pictorially a two-dimensional array of sensor arrays as shown in Fig. 5 mounted in side-to-side relationship so as to form a composite detector; after completion of the second manufacturing step;

Fig. 7 shows pictorially a third manufacturing step according to the invention for depositing sensor material on the top side of the detector;

Fig. 8 shows pictorially a detector formed of multiple two-dimensional sensor arrays according to the invention commonly mounted on a printed circuit board, after completion of the third manufacturing step;

Fig. 9 shows pictorially an arcuate detector formed of multiple two-dimensional sensor arrays according to the invention commonly mounted on a printed circuit board; and

Fig. 10 is a flow diagram summarizing the manufacturing process of a sensor array according to the invention.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS

Fig. 3 shows pictorially an exploded view of a silicon wafer 30 constituting an integrated circuit or chip, typically formed of a complementary metal oxide semiconductor (CMOS) wafer comprising a large area rectangular matrix of sensor

elements or pixels 31. The wafer 30 is processed at a silicon foundry to yield multiple replicas of the same integrated circuit. Each pixel 31 includes a sensor input 32 that is connected to a charge amplifier 33 and a processing unit 34. The charge amplifier 33 together with the processing unit 34 constitute the pixel electronics to which the sensor element (not shown) is connected and which responds to a photon striking the sensor element for measuring the charge produced thereby. Thus, the silicon wafer 30 contains a very large array of electronic circuits for connecting to a respective sensor element. Control connections to each sensor pixel are made via connections that are routed on the wafer to a controller 35 fabricated at an edge thereof and having terminal pads that serve as I/O ports to the IC. In order that a relatively small number of terminal pads may interface to the very large number of pixels in the complete wafer, the controller 35 includes a multiplexer (not shown) that allows the terminal pads to address any selected sensor element in known manner. Such an approach obviates the need to provide conductive vias through the wafer as is done in PCT/IL03/00125.

Fig. 4 shows a complete sensor array 40, also referred to as a "pixel stick", having an overall length (L) that may exceed 10cm and whose width (W) is typically in the order of 1cm. In order to fabricate a wafer having a very large area, while minimizing failures, an artwork of conventional size corresponding to a pixel array having, for example, 256 pixels is repetitively projected on to the CMOS wafer and processed so as form in a stepped manner a complete wafer having greatly increased area. This technique is known as "stitching" and is described, for example in "*A 35mm 13.89 million pixel CMOS active pixel sensor*" by G. Meynants *et al.*, IEEE Workshop on CCD & AIS, May 15-17, 2003. The same technique, albeit in a different context, is described and illustrated in "*1,024 x 1,024 Resistive Emitter ArrayDesign & Fabrication Status*" by Paul Bryant *et al.*, Santa Barbara Infrared, Inc.

Figs. 5 and 6 show pictorially a detector 50 formed by juxtaposing a plurality of sensor arrays 40, respectively prior to and after completing a second manufacturing step. The CMOS wafer in each sensor array has a major edge and a minor

edge, the major edge having a dimension (L) that is no less than approximately half of the required width of the detector. Multiple pairs of sensor arrays 40 edge to edge so that respective minor edges of each of pair are juxtaposed with the respective terminal pads 35 of each sensor array disposed toward opposing outer non-contiguous edges of the detector 50 and with adjacent pairs of sensor arrays being juxtaposed along their major edges. By such means, the terminal pads 35 are disposed toward opposing outermost edges of the detector 50 and constitute the only "dead space" in the detector since there are no terminal pads between adjoining edges of the detector.

Referring to Fig. 7 there is shown a subsequent stage in the manufacturing process where desired amorphous or polycrystalline sensor material such as mercury iodide is grown on the top side of the wafers of the assembled detector 50 so as to form an array of diodes, each having a first electrode which is in ohmic contact with a respective one of the sensor inputs 32 (shown in Fig. 3) and such that the opposite, exposed, surface of the sensor material forms a common second electrode of opposite polarity to that of the first electrode towards which incident photons are directed. Typically, the first electrode serves as the anode and the second electrode as the cathode, but this may be reversed depending on how the IC is biased.

Fig. 8 shows pictorially a composite detector 55 after completion of the deposition process having a lower assembly of silicon sensor arrays 40 as described above and shown in Figs. 4 and 5, on top of which is grown a sensor layer 56 of amorphous or polycrystalline sensor material such as mercury iodide so as to form a large matrix of sensor elements having a common cathode constituted by the upper surface of the device and a respective anode (not shown) that is effectively sandwiched between the sensor layer 56 and the lower wafer of the silicon sensor arrays 40 and is connected via a corresponding one of the sensor inputs 32 formed in the silicon wafer 30, shown in Fig. 3. The resulting assembly is mounted on a ceramic PCB 57 to which the terminal pads of each controller are connected via wire bonds 57. In practice, the PCB 57 is connected to an external data controller

and power supplies as known in the art and preferably the IC(s) are mounted on the PCB 57 before the deposition of the sensor material.

Fig. 9 shows pictorially an arcuate detector 60 formed of multiple two-dimensional sensor arrays 40 according to the invention commonly mounted on a printed circuit board 61 and covered with the deposited sensor layer 56, as shown in Fig. 8. The terminal pads 35 are toward opposing outermost edges of the detector 60 and constitute the only "dead space" in the detector since there are no terminal pads between adjoining edges of the constituent sensor arrays. The length of the detector can be increased as required by juxtaposing more pairs of sensor arrays, but the width of the detector is always double the length (L) of a single sensor array. Currently, as noted above, the length (L) of a single sensor array is in the order of 10cm resulting in a detector width in the order of 20cm but this will undoubtedly increase as manufacturing techniques improve and is predicted to reach the width of a conventional CT scanner within a few years. This means that for the first time it is possible to manufacture a CT detector having effectively no dead space since, as noted above, providing incident X-rays (for example) are not directed on the outermost edges of the detector there is no dead space between adjoining sensor arrays. In practice, a large area curved PCB is more likely to be formed as a juxtaposition of planar PCB segments.

Fig. 10 is a flow diagram summarizing the essential features of the above-described manufacturing process of a detector according to the invention, wherein a very large area integrated circuit is formed having at least one array of electronic processing circuits each having a respective sensor input that is accessible from a first surface of the integrated circuit. Amorphous or polycrystalline sensor material is then deposited on the upper surface of the wafer (constituting a first surface) so as to form an array of diodes, each having a first electrode which is in ohmic contact with a respective one of the sensor inputs and such that the exposed surface of the sensor material forms a common second electrode of opposite polarity to the first electrode towards which incident photons are directed.

Whilst, in the preferred embodiment as described above, the sensor elements are themselves grown using mercury iodide on to the silicon wafer, it will be appreciated that other polycrystalline materials may be used such as amorphous selenium and lead iodide. In all such cases, the sensor material is deposited on top of the wafer in contact with the sensor inputs as described in the preferred embodiment. However, the invention also contemplates the use of crystalline materials such as cadmium zinc telluride, gallium arsenide and cadmium mercury iodide. These are not grown on the wafer but are grown separately to form flat panels that are then deposited on the upper surface of the wafer with each sensor element in registration with a corresponding sensor input and connected thereto via bump bonding. Thus the invention also contemplates the situation where the sensor elements and the sensor electronics are formed in discrete layers, which are bonded together rather than being formed as a monolithic structure. In saying this, it is to be noted that bump-bonding is expensive, which is why polycrystalline deposition is a much more low-cost, and thereby better, approach. In all cases, the invention avoids the need for vias as taught in our PCT/IL03/00125 and the other prior art references discussed above.

Although use of such sensors in X-ray and γ-ray imaging systems has been mentioned, it is to be noted that the invention is not limited to any particular application. Thus, other applications of the invention will be apparent to one skilled in the art and include, without limitation, X-ray computed tomography; night vision sensors; standard medical and industrial X-ray devices; nuclear medicine PET/SPECT sensors; particle detectors; X-ray diffraction detectors and others.

In the preferred embodiment, the electronic processing circuits include amplifiers and further processing circuitry. This allows incident photons to threshold charge the pixel array and to be counted on impact. However, this also is not intended to limit the invention since at their most basic the electronic processing circuits can be simply capacitors that store the incoming charge, in a manner somewhat analogous to a CCD, where charge is read out sequentially similar to a shift register.

It should also be noted that in CMOS technology, the CMOS layer is covered by an insulating layer of silicon oxide, which must be removed if a circuit element is to be exposed in order to allow actual electrical connection thereto. Since in the invention, the sensor elements are deposited on the upper surface of the wafer, the sensor inputs must first be exposed to allow electrical connection of the sensor elements.

Finally, it is to be noted that while the invention has been described with particular reference of the fabrication and assembly of a detector having a plurality of sensor arrays, the sensor array is clearly an essential component of such a detector assembly and could be provided independent of the detector assembly. In such case, there are essentially two possibilities for depositing the sensor material. Manufacturers of mercury iodide generally recommend that the complete area of the detector be deposited with sensor material so as to cover all component sensor arrays thereof, since this reduces artifacts that can form at the edges of adjacent sensor arrays if the sensor material is deposited on the sensor arrays before assembly. This would tend to militate against the provision of sensor arrays on which sensor material had already been deposited for assembly on to a PCB by an independent party; and would favor the sensor arrays being supplied without the sensor material. The sensor arrays would then be assembled on to a PCB by an independent party who would then deposit the sensor material as described above.

CLAIMS:

1. A method for fabricating a detector assembly having multiple juxtaposed sensor arrays each having a plurality of pixels that include a sensor element coupled to a sensor input of an electronic processing circuit, the method comprising:

integrating the electronic processing circuits on a very large area CMOS wafer having a major edge and a minor edge, the major having a dimension that is no less than approximately half of a width of the detector so as to form an integrated circuit having at least one array of electronic processing circuits each electronic processing circuit having a respective sensor input disposed toward a first surface of the wafer and accessible from the first surface via a contact formed towards a minor edge of the sensor array;

juxtaposing multiple pairs of sensor arrays edge to edge so that respective minor edges of each of pair are juxtaposed with the respective contacts of each sensor array disposed toward opposing outer non-contiguous edges of the detector and with adjacent pairs of sensor arrays being juxtaposed along their major edges; and

disposing the sensor elements on the first surface of the respective integrated circuits in said detector assembly whereby an exposed surface of the sensor elements forms a common first electrode towards which incident photons are directed, and an opposite unexposed surface thereof forms multiple second electrodes of opposite polarity to the first electrode each in registration with a corresponding sensor input.

2. The method according to claim 1, wherein disposing the sensor elements includes growing amorphous or polycrystalline sensor material on the first surface of the wafer.

3. The method according to claim 2, wherein the detector assembly is mounted on a PCB prior to disposing the sensor elements.

4. The method according to claim 1, wherein disposing the sensor elements includes mounting monolithically integrated crystalline sensors on the first surface of the wafer in registration with respective sensor inputs.

5. The method according to claim 4, wherein the sensor elements are connected to the sensor inputs via bump bonding.

6. The method according to any one of claims 1 to 5, when used to fabricate a sensor array for a high energy photon imaging detector.

7. A detector assembly manufactured according to any one of Claims 1 to 6.

8. A detector assembly having multiple juxtaposed sensor arrays each having a plurality of pixels that include a sensor element coupled to a sensor input of an electronic processing circuit, the detector assembly comprising:

a plurality of sensor arrays each fabricated on a very large area CMOS wafer having a major edge and a minor edge, the major having a dimension that is no less than approximately half of a width of the detector and forming an integrated circuit having at least one array of electronic processing circuits each electronic processing circuit having a respective sensor input disposed toward a first surface of the wafer and accessible from the first surface via a contact formed towards a minor edge of the sensor array;

multiple pairs of sensor arrays juxtaposed edge to edge so that respective minor edges of each of pair are juxtaposed with the respective contacts of each sensor array disposed toward opposing outer non-contiguous edges of the detector and with adjacent pairs of sensor arrays being juxtaposed along their major edges; and

sensor elements disposed on the first surface of the respective integrated circuits in said detector assembly whereby an exposed surface of the sensor elements forms a common first electrode towards which incident photons are directed, and an opposite unexposed surface thereof forms multiple second electrodes of opposite polarity to the first electrode each in registration with a corresponding sensor input.

9. The detector assembly according to claim 8, wherein the sensor elements include amorphous or polycrystalline sensor material grown on the first surface of the wafer.

10. The detector assembly according to claim 8, wherein the sensor elements include monolithically integrated crystalline sensors mounted on the first surface of the wafer in registration with respective sensor inputs.

11. The detector assembly according to any one of claim 8 to 10, being configured for use in a high energy photon imaging detector.

12. A sensor array for use in manufacture of the detector assembly according to any one of claims 8 to 11, the sensor array comprising:

a very large area CMOS wafer having a major edge and a minor edge, the major having a dimension that is no less than approximately half of a width of the detector and forming an integrated circuit having at least one array of electronic processing circuits each electronic processing circuit having a respective sensor input disposed toward a first surface of the wafer and accessible from the first surface via a contact formed towards a minor edge of the sensor array.

13. The sensor array according to claim 12, further including sensor material deposited on the first surface thereof.

For the Applicants,
REINHOLD COHN AND PARTNERS
By:

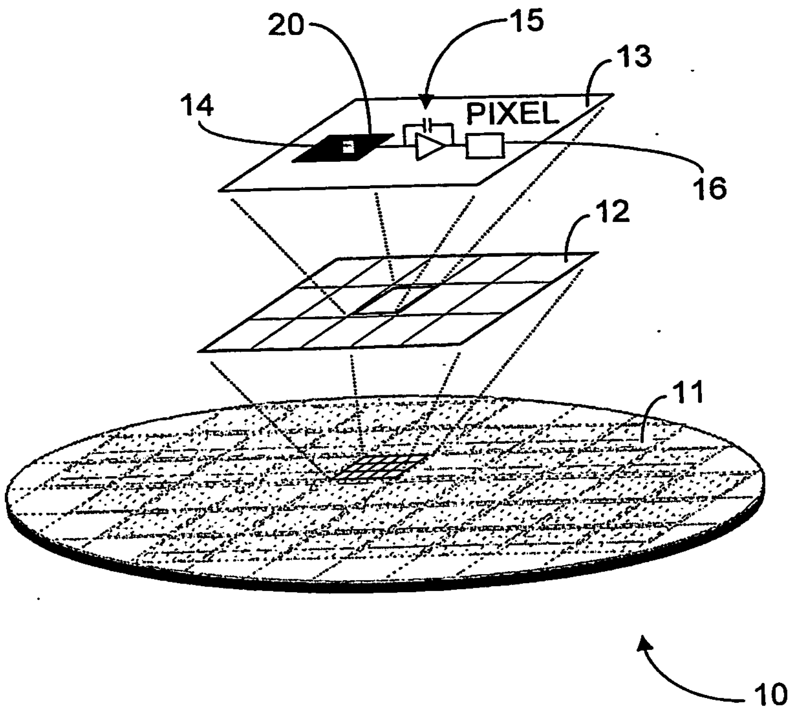

FIG. 1
(PRIOR ART)

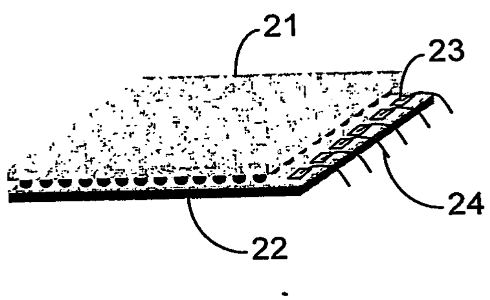

FIG. 2
(PRIOR ART)

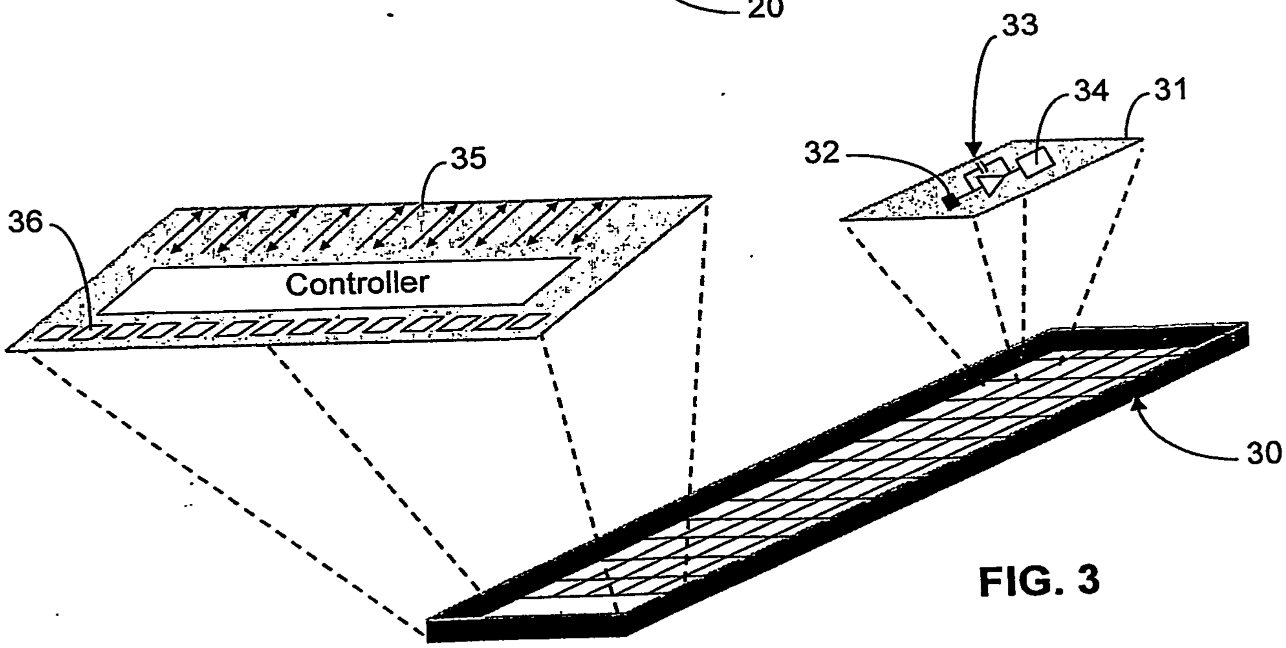

FIG. 3

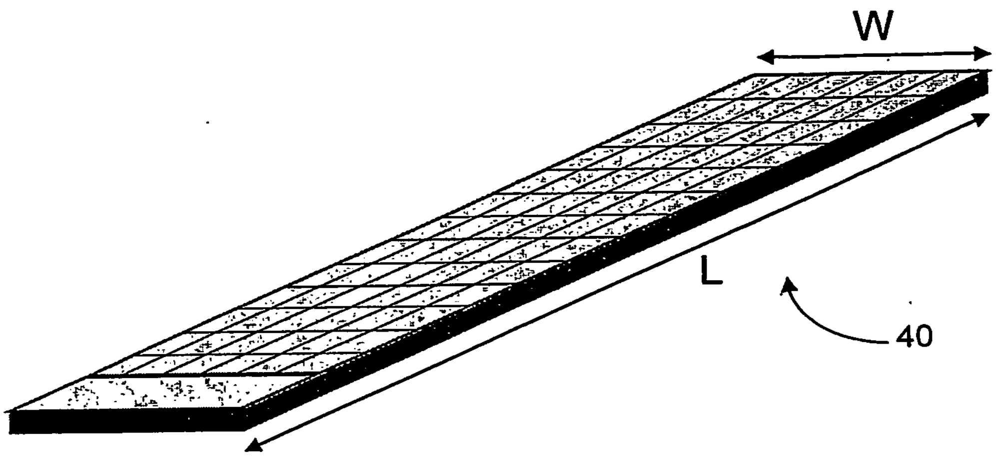

FIG. 4

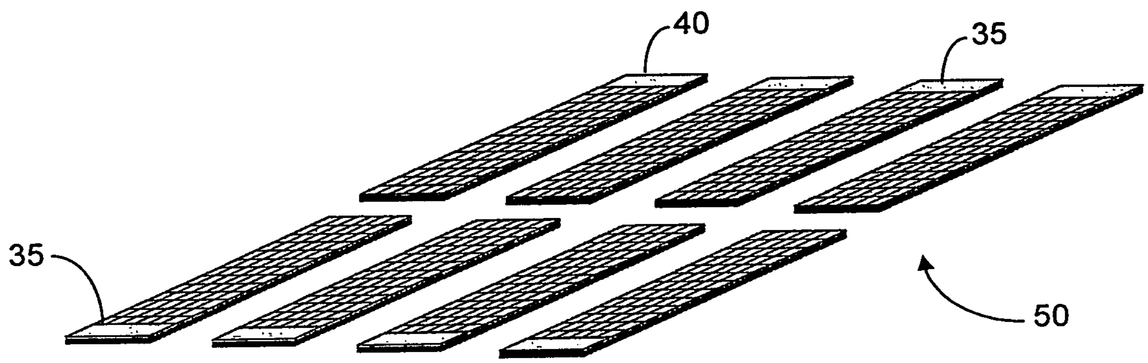

FIG. 5

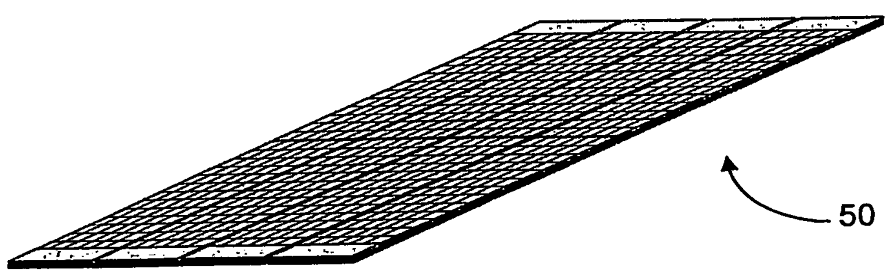

FIG. 6

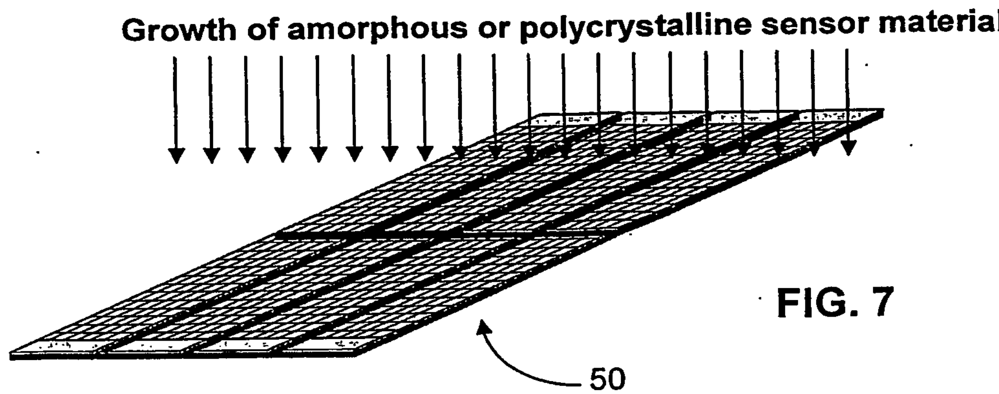

FIG. 7

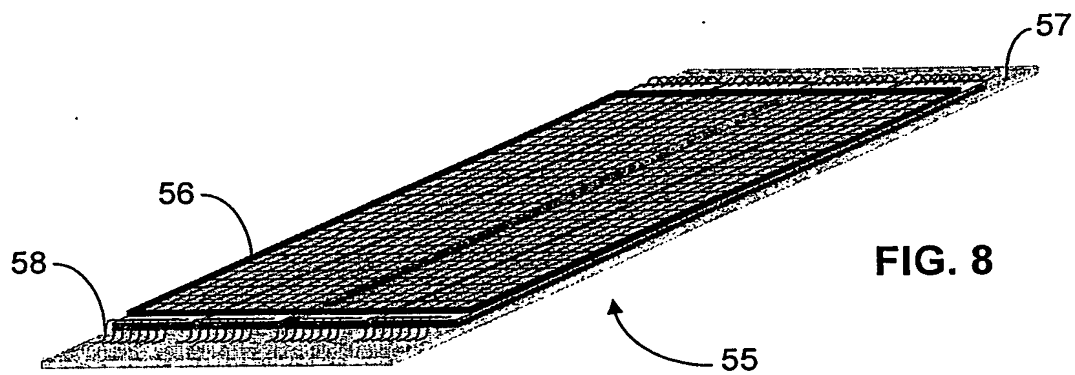

FIG. 8

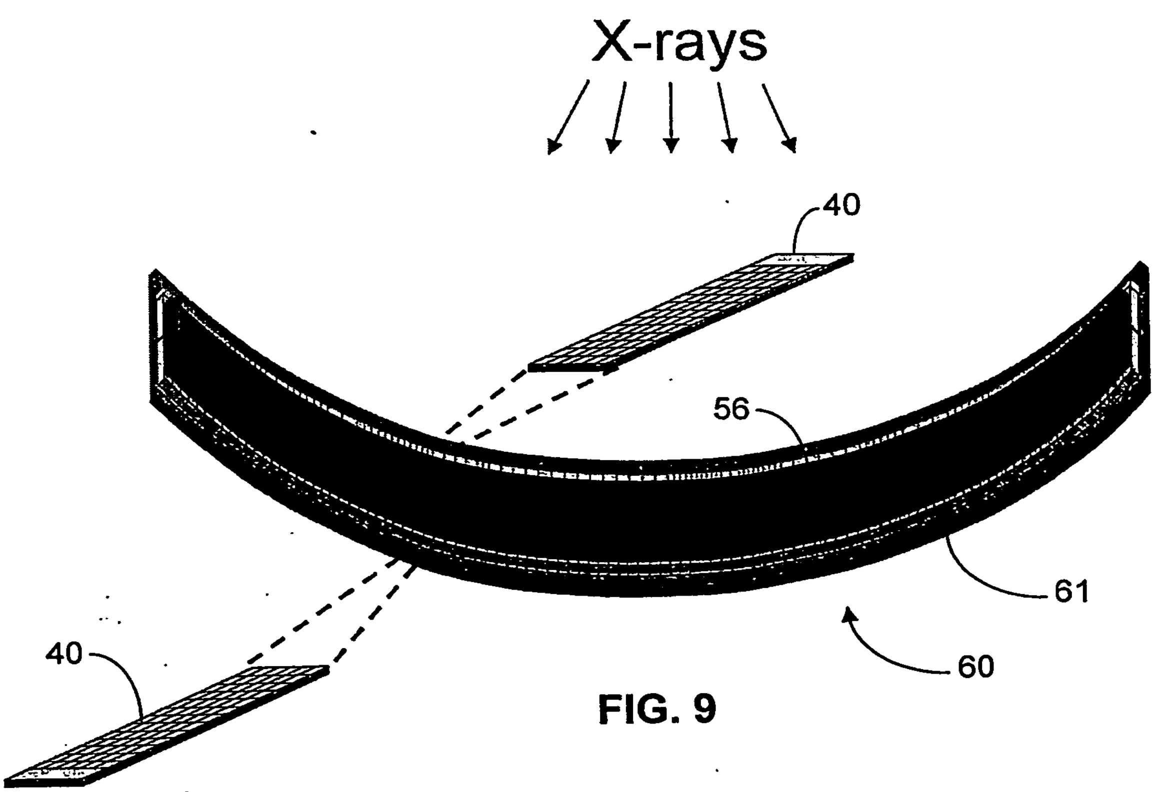

FIG. 9

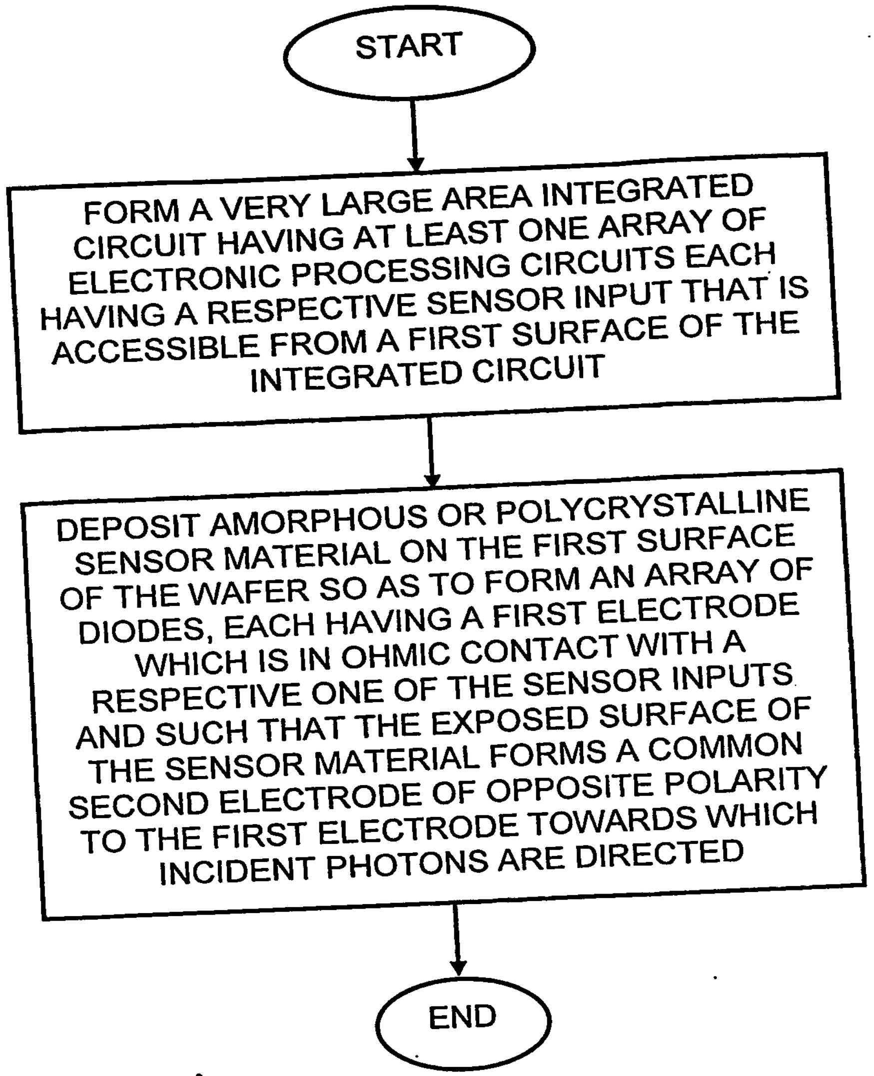
START
FORM A VERY LARGE AREA INTEGRATED CIRCUIT HAVING AT LEAST ONE ARRAY OF ELECTRONIC PROCESSING CIRCUITS EACH HAVING A RESPECTIVE SENSOR INPUT THAT IS ACCESSIBLE FROM A FIRST SURFACE OF THE INTEGRATED CIRCUIT
DEPOSIT AMORPHOUS OR POLYCRYSTALLINE SENSOR MATERIAL ON THE FIRST SURFACE OF THE WAFER SO AS TO FORM AN ARRAY OF DIODES, EACH HAVING A FIRST ELECTRODE WHICH IS IN OHMIC CONTACT WITH A RESPECTIVE ONE OF THE SENSOR INPUTS AND SUCH THAT THE EXPOSED SURFACE OF THE SENSOR MATERIAL FORMS A COMMON SECOND ELECTRODE OF OPPOSITE POLARITY TO THE FIRST ELECTRODE TOWARDS WHICH INCIDENT PHOTONS ARE DIRECTED
END

FIG. 10

Document made available under the Patent Cooperation Treaty (PCT)

International application number: PCT/IL04/000915

International filing date: 04 October 2004 (04.10.2004)

Document type: Certified copy of priority document

Document details: Country/Office: IL
Number: 158345
Filing date: 09 October 2003 (09.10.2003)

Date of receipt at the International Bureau: 07 December 2004 (07.12.2004)

Remark: Priority document submitted or transmitted to the International Bureau in compliance with Rule 17.1(a) or (b)